non-display region in a direction perpendicular to the substrate, thereby further realizing the narrow-frame design.

[0046] Although some embodiments and the applied technology principles of the present disclosure have been described as above, it should be understood by those skilled in the art that the present disclosure is not limited to particular embodiments described herein. Various modifications, readjustment and alternations can be made by those skilled in the art without departing the scope of protection of the present disclosure, and these modifications, readjustment and alternations fall within the scope of the present disclosure which is subject to the appended claims.

1. An array substrate, comprising:

a substrate comprising a display region and a non-display region, wherein the display region comprises a plurality of gate lines, a plurality of data lines and a plurality of touch leads; and

a plurality of touch electrodes insulated from each other, with each of the plurality of touch electrodes being electrically connected to a respective one of the plurality of touch leads; and, wherein the non-display region comprises:

a first polar plate of a first capacitor, a second polar plate of the first capacitor and a first signal bus, wherein

the first capacitor is formed by overlapping the first polar plate of the first capacitor with the second polar plate of the first capacitor in a direction perpendicular to the substrate, and

the first signal bus is partially overlapped with the first polar plate of the first capacitor and the second polar plate of the first capacitor in the direction perpendicular to the substrate.

2. The array substrate of claim **1**, wherein the first polar plate of the first capacitor and the gate lines are manufactured in a same layer, the second polar plate of the first capacitor and the data lines are manufactured in a same layer, and the first signal bus and the touch leads are manufactured in a same layer.

3. The array substrate of claim **2**, further comprising a first insulation layer and a second insulation layer, wherein the first insulation layer is provided between the first polar plate of the first capacitor and the second polar plate of the first capacitor, and the second insulation layer is provided between the first signal bus and the second polar plate of the first capacitor.

4. The array substrate of claim **3**, wherein

the first insulation layer has a first through-hole, the second insulation layer has a second through-hole, and the first through-hole and the second through-hole jointly form a third through-hole which exposes a portion of the first polar plate of the first capacitor, and

the first signal bus is electrically connected to the first polar plate of the first capacitor through the third through-hole.

5. The array substrate of claim **3**, wherein the second insulation layer has a second through-hole which exposes a portion of the second polar plate of the first capacitor, and the first signal bus is electrically connected to the second polar plate of the first capacitor through the second through-hole.

6. The array substrate of claim **1**, further comprising a first polar plate of a second capacitor, a second polar plate of the second capacitor and a second signal bus, wherein

the second capacitor is formed by overlapping the first polar plate of the second capacitor with the second polar plate of the second capacitor in a direction perpendicular to the substrate, and

the second signal bus is partially overlapped with the first polar plate of the second capacitor and the second polar plate of the second capacitor in the direction perpendicular to the substrate.

7. The array substrate of claim **6**, further comprising a first insulation layer and a second insulation layer, wherein the first polar plate of the first capacitor is electrically insulated from the first polar plate of the second capacitor, and the second polar plate of the first capacitor is electrically insulated from the second polar plate of the second capacitor, wherein

the first insulation layer is provided between the first polar plate of the first capacitor and the second polar plate of the first capacitor and between the first polar plate of the second capacitor and the second polar plate of the second capacitor, and

the second insulation layer is provided between the first signal bus and the second polar plate of the first capacitor and between the second signal bus and the second polar plate of the second capacitor.

8. The array substrate of claim **7**, wherein

the first insulation layer has a first through-hole, the second insulation layer has a second through-hole, and the first through-hole and the second through-hole jointly form a third through-hole which exposes a portion of the first polar plate of the second capacitor, and

the second signal bus is electrically connected to the first polar plate of the second capacitor through the third through-hole.

9. The array substrate of claim **7**, wherein

the second insulation layer has a second through-hole, the second through-hole exposes a portion of the second polar plate of the second capacitor, and

the second signal bus is electrically connected to the second polar plate of the second capacitor through the second through-hole.

10. The array substrate of claim **6**, wherein the first signal bus, the second signal bus and the touch leads are all made of metal materials.

11. The array substrate of claim **10**, wherein

a pattern of the first polar plate of the first capacitor, a pattern of the second polar plate of the first capacitor, and a pattern of the first signal bus are the same,

projections of the first polar plate of the first capacitor and the second polar plate of the first capacitor are completely overlapped with a projection of the first signal bus in a direction perpendicular to the substrate,

a pattern of the first polar plate of the second capacitor, a pattern of the second polar plate of the second capacitor, and a pattern of the second signal bus are the same, and

projections of the first polar plate of the second capacitor and the second polar plate of the second capacitor are completely overlapped with a projection of the second signal bus in a direction perpendicular to the substrate.

12. The array substrate of claim **6**, wherein the gate lines and data lines are both made of metal, and the first signal bus, the second signal bus and the touch leads are made of